SGS-THOMSON MICROELECTRONICS

IMS C011E

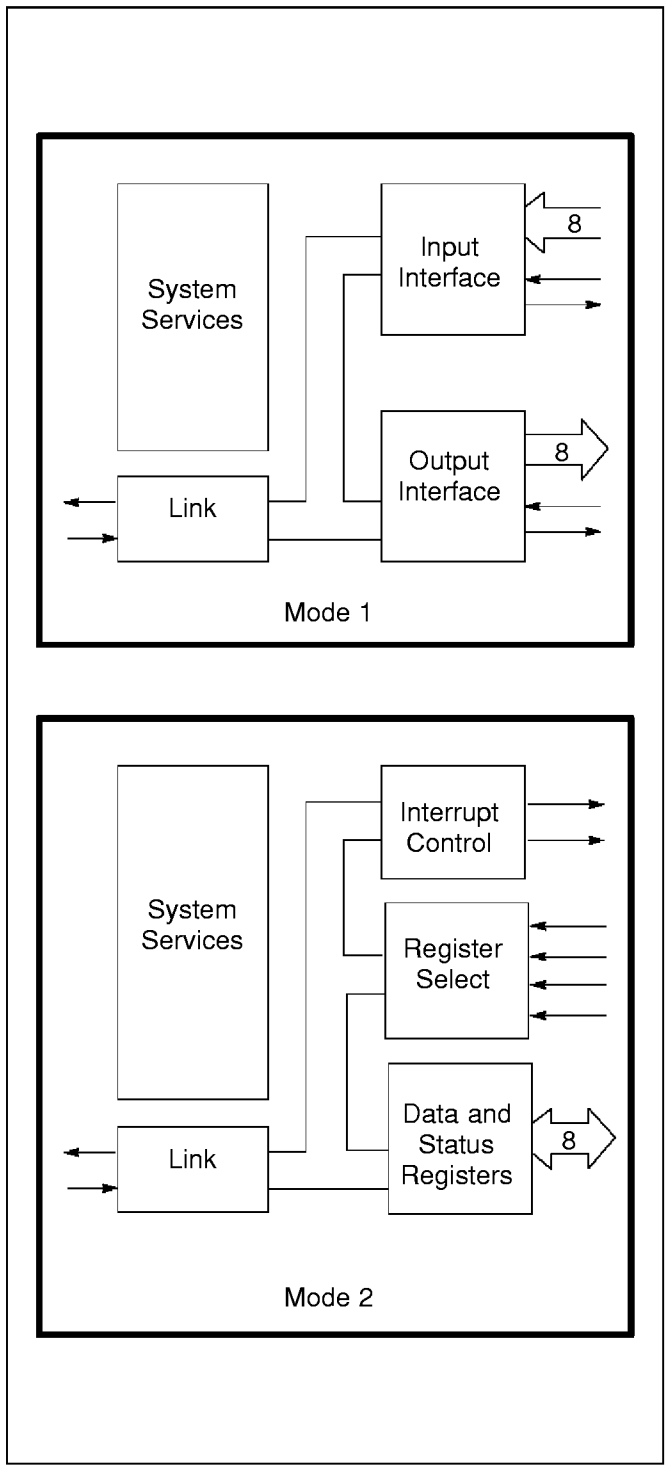
Link adaptor – Extended temperature

FEATURES

- Standard INMOS link protocol
- 10 or 20 Mbits/sec operating speed
- Communicates with transputers
- Converts between serial link and parallel bus
- Converts between serial link and parallel device
- Two modes of parallel operation:
  - **Mode 1: Peripheral interface**
    - Eight bit parallel input interface
    - Eight bit parallel output interface
    - Full handshake on input and output
  - **Mode 2: Bus interface**
    - Tristate bidirectional bus interface
    - Memory mapped registers
    - Interrupt capability
- Single +5V 5% power supply
- TTL and CMOS compatibility
- 150mW power dissipation
- 28 pin 0.6" DIL package
- 28 pin LCCC package
- Extended operating temperature –55_C to +125_C

APPLICATIONS

- Programmable I/O for transputer
- Connecting microprocessors to transputers
- High speed links between microprocessors
- Inter-family microprocessor interfacing
- Interconnecting different speed links



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Contents

1 Introduction

The INMOS communication link is a high speed system interconnect which provides full duplex communication between members of the transputer family, according to the INMOS serial link protocol. The IMS C011E, a member of this family, provides for full duplex transputer link communication with standard microprocessor and sub-system architectures, by converting bi-directional serial link data into parallel data streams.

All products which use INMOS communication links, regardless of device type, support a standard communications frequency of 10 Mbits/sec; most products also support 20 Mbits/sec. Products of different type or performance can, therefore, be interconnected directly and future systems will be able to communicate directly with those of today. The IMS C011E link will run at either the standard speed of 10 Mbits/sec or at the higher speed of 20 Mbits/sec. Data reception is asynchronous, allowing communication to be independent of clock phase.

The link adaptor can be operated in one of two modes. In Mode 1 the IMS C011E converts between a link and two independent fully handshaken byte-wide interfaces, one input and one output. It can be used by a peripheral device to communicate with a transputer, a peripheral processor or another link adaptor, or it can provide programmable input and output pins for a transputer. Two IMS C011E devices in this mode can be connected back to back via the parallel ports and used as a frequency changer between different speed links.

In Mode 2 the IMS C011E provides an interface between an INMOS serial link and a microprocessor system bus. Status and data registers for both input and output ports can be accessed across the byte-wide bi-directional interface. Two interrupt outputs are provided, one to indicate input data available and one for output buffer empty.

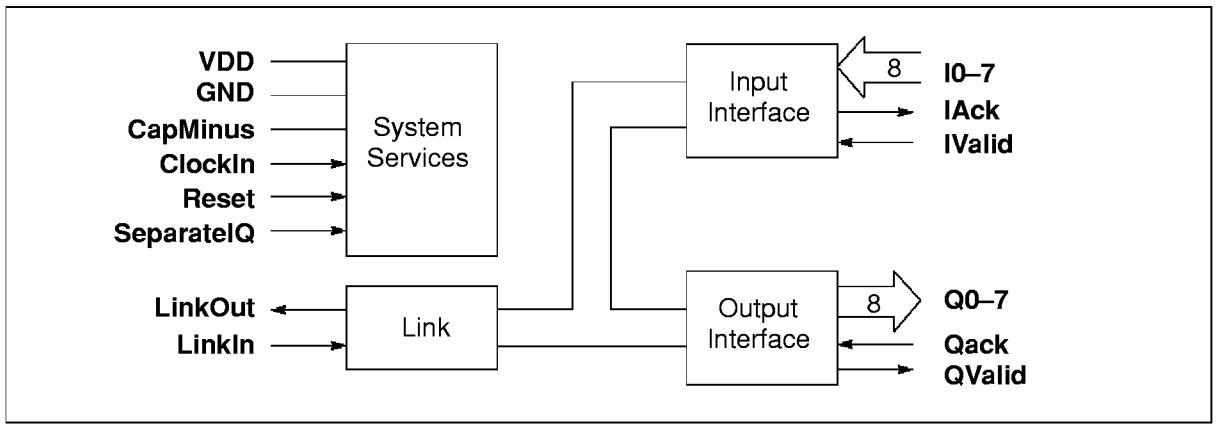


Figure 1.1 IMS C011E Mode 1 block diagram

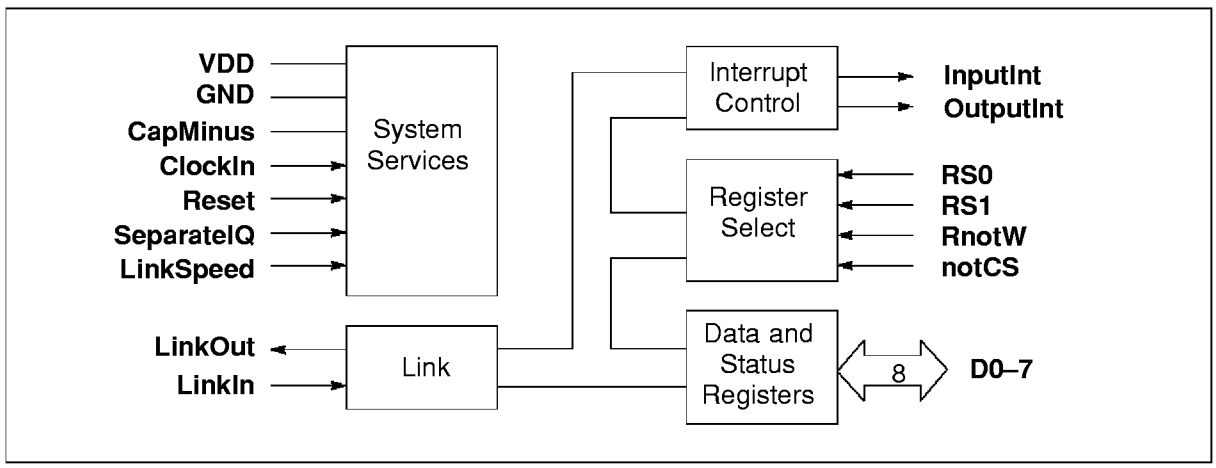


Figure 1.2 IMS C011E Mode 2 block diagram

2 Pin designations

Signal names are prefixed by **not** if they are active low, otherwise they are active high.
Pinout details for various packages are given in section 8.

Pin	In/Out	Function
VDD, GND		Power supply and return
CapMinus		External capacitor for internal clock power supply
ClockIn	in	Input clock
Reset	in	System reset
SeparateIQ	in	Select mode and Mode 1 link speed
LinkIn	in	Serial data input channel
LinkOut	out	Serial data output channel

Table 2.1 Services and link

Pin	In/Out	Function
I0-7	in	Parallel input bus
IValid	in	Data on **I0-7** is valid
IAck	out	Acknowledge **I0-7** data received by other link
Q0-7	out	Parallel output bus
QValid	out	Data on **Q0-7** is valid
QAck	in	Acknowledge from device: data **Q0-7** was read

Table 2.2 Mode 1 parallel interface

Pin	In/Out	Function
D0-7	in/out	Bi-directional data bus
notCS	in	Chip select
RS0-1	in	Register select
RnotW	in	Read/write control signal
InputInt	out	Interrupt on link receive buffer full
OutputInt	out	Interrupt on link transmit buffer empty
LinkSpeed	in	Select link speed as 10 or 20 Mbits/sec
HoldToGND		Must be connected to **GND**
DoNotWire		Must not be wired

Table 2.3 Mode 2 parallel interface

3 System services

System services include all the necessary logic to start up and maintain the IMS C011E.

3.1 Power

Power is supplied to the device via the **VDD** and **GND** pins. The supply must be decoupled close to the chip by at least one 100 nF low inductance (e.g. ceramic) capacitor between **VDD** and **GND**. Four layer boards are recommended; if two layer boards are used, extra care should be taken in decoupling.

AC noise between **VDD** and **GND** must be kept below 200 mV peak to peak at all frequencies above 100 KHz. AC noise between **VDD** and the ground reference of load capacitances must be kept below 200 mV peak to peak at all frequencies above 30 MHz. Input voltages must not exceed specification with respect to **VDD** and **GND**, even during power-up and power-down ramping, otherwise *latchup* can occur. CMOS devices can be permanently damaged by excessive periods of latchup.

3.2 CapMinus

The internally derived power supply for internal clocks requires an external low leakage, low inductance 1nF capacitor to be connected between **VDD** and **CapMinus**. A ceramic capacitor is preferred, with an impedance less than 3 Ohms between 100 KHz and 10 MHz. If a polarized capacitor is used the negative terminal should be connected to **CapMinus**. Total PCB track length should be less than 50 mm. The positive connection of the capacitor must be connected directly to **VDD**. Connections must not otherwise touch power supplies or other noise sources.

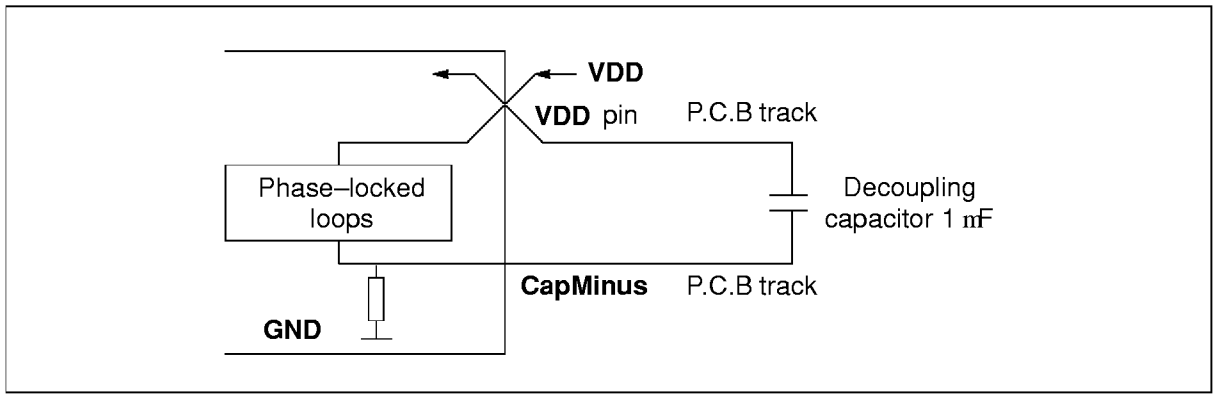


Figure 3.1 Recommended PLL decoupling

3.3 ClockIn

Transputer family components use a standard clock frequency, supplied by the user on the **ClockIn** input. The nominal frequency of this clock for all transputer family components is 5 MHz, regardless of device type, transputer word length or processor cycle time. High frequency internal clocks are derived from **ClockIn**, simplifying system design and avoiding problems of distributing high speed clocks externally.

A number of transputer family devices may be connected to a common clock, or may have individual clocks providing each one meets the specified stability criteria. In a multi-clock system the relative phasing of **ClockIn** clocks is not important, due to the asynchronous nature of the links. Mark/space ratio is unimportant provided the specified limits of **ClockIn** pulse widths are met.

Oscillator stability is important. **ClockIn** must be derived from a crystal oscillator; RC oscillators are not sufficiently stable. **ClockIn** must not be distributed through a long chain of buffers. Clock edges must be monotonic and remain within the specified voltage and time limits.

Symbol	Parameter	Min	Nom	Max	Units	Notes
TDCLDCH	**ClockIn** pulse width low	40			ns	
TDCHDCL	**ClockIn** pulse width high	40			ns	
TDCLDCL	**ClockIn** period		200		ns	1,3
TDCerror	**ClockIn** timing error			0.5	ns	2
TDC1DC2	Difference in **ClockIn** for 2 linked devices			400	ppm	3
TDCr	**ClockIn** rise time			10	ns	4
TDCf	**ClockIn** fall time			8	ns	4

Notes

1 Measured between corresponding points on consecutive falling edges.

2 Variation of individual falling edges from their nominal times.

3 This value allows the use of 200ppm crystal oscillators for two devices connected together by a link.

4 Clock transitions must be monotonic within the range **VIH** to **VIL** (table 7.3).

Table 3.1 Input clock

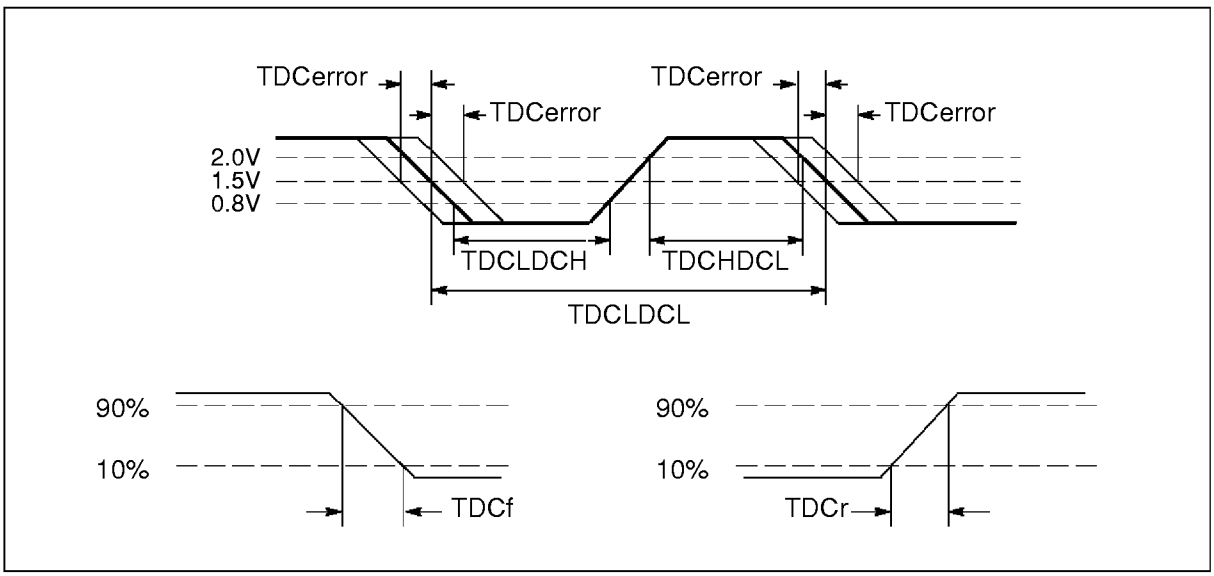


Figure 3.2 ClockIn timing

3.4 SeparateIQ

The IMS C011E link adaptor has two different modes of operation. Mode 1 is basically a link to peripheral adaptor, whilst Mode 2 interfaces between a link and a microprocessor bus system.

Mode 1 can be selected for one of two link speeds by connecting **SeparateIQ** to **VDD** (10 Mbits/sec) or to **ClockIn** (20 Mbits/sec).

Mode 2 is selected by connecting **SeparateIQ** to **GND**; in this mode 10 Mbits/sec or 20 Mbits/sec is selected by **LinkSpeed**. Link speeds are specified for a **ClockIn** frequency of 5 MHz.

In order to select the link speed, **SeparateIQ** may be changed dynamically providing the link is in a quiescent state and no input or output is required. **Reset** must be applied subsequent to the selection to initialize the device. If **ClockIn** is gated to achieve this, its skew must be limited to the value **TDCHSIQH** shown in table 3.3. The mode of operation (Mode 1, Mode 2) must not be changed dynamically.

SeparateIQ	Mode	Link Speed Mbits/sec
VDD	1	10
ClockIn	1	20
GND	2	10 or 20

Table 3.2 **SeparateIQ** mode selection

Symbol	Parameter	Min	Nom	Max	Units	Notes
TDCHSIQH	Skew from **ClockIn** to **ClockIn**			20	ns	1

Notes

1 Skew between **ClockIn** arriving on the **ClockIn** pin and on the **SeparateIQ** pin.

Table 3.3 **SeparateIQ**

3.5 Reset

The **Reset** pin can go high with **VDD**, but must at no time exceed the maximum specified voltage for **VIH**. After **VDD** is valid **ClockIn** should be running for a minimum period **TDCVRL** before the end of **Reset**. All inputs, with the exception of **ClockIn** and **SeparateIQ** (plus **LinkSpeed** in mode 2), must be held in their inactive state during reset.

Reset initializes the IMS C011E to the following state: **LinkOut** is held low; the control outputs (**IAck** and **QValid** in Mode 1, **InputInt** and **OutputInt** in Mode 2) are held low; interrupts (Mode 2) are disabled; the states of **Q0-7** in Mode 1 are unspecified; **D0-7** in Mode 2 are high impedance.

Symbol	Parameter	Min	Nom	Max	Units	Notes
TPVRH	Power valid before **Reset**	10			ms	1
TRHRL	**Reset** pulse width high	8			ClockIn	1,2
TDCVRL	**ClockIn** running before **Reset** end	10			ms	1,3
TRLIvH	**Reset** low before **IValid** high (mode 1)	0			ns	1
TRLCSL	**Reset** low before chip select low (mode 2)	0			ns	1

Notes

1 This parameter is not tested.

2 Full periods of **ClockIn TDCLDCL** required.

3 At power-on reset.

Table 3.4 Reset

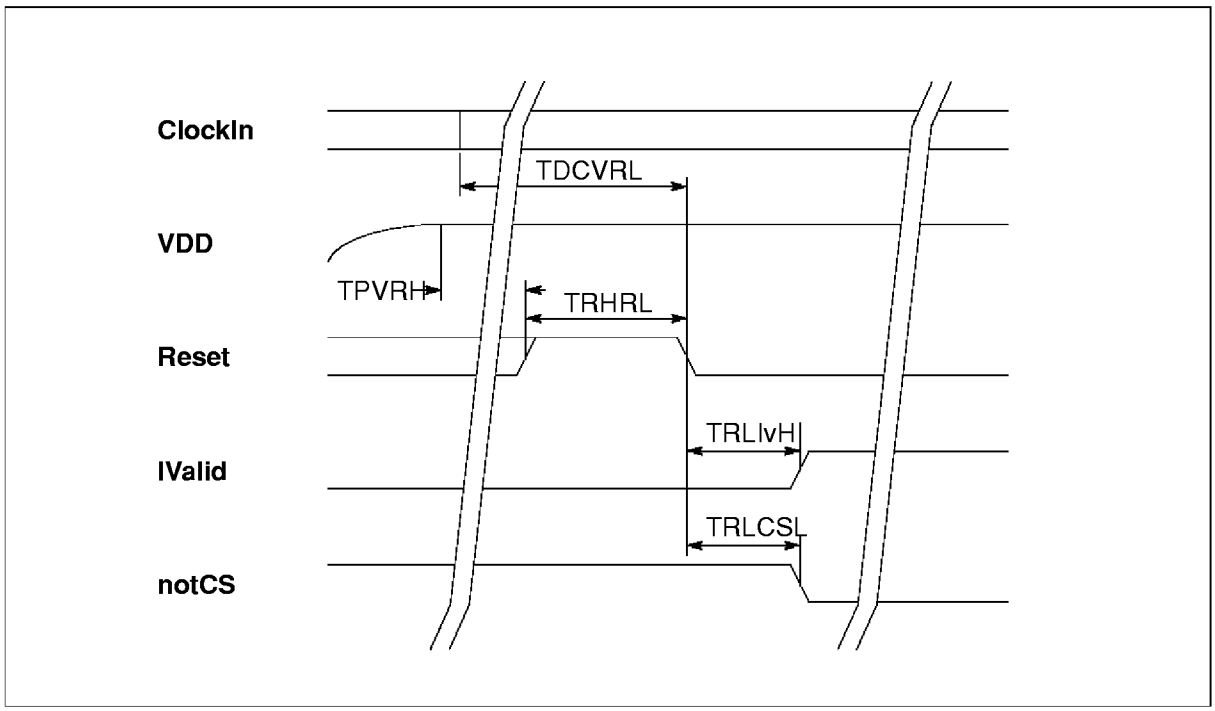


Figure 3.3 **Reset** timing

4 Links

INMOS bi-directional serial links provide synchronized communication between transputer products and with the outside world. Each link comprises an input channel and output channel. A link between two devices is implemented by connecting a link interface on one device to a link interface on the other device. Every byte of data sent on a link is acknowledged on the input of the same link, thus each signal line carries both data and control information.

The quiescent state of a link output is low. Each data byte is transmitted as a high start bit followed by a one bit followed by eight data bits followed by a low stop bit. The least significant bit of data is transmitted first. After transmitting a data byte the sender waits for the acknowledge, which consists of a high start bit followed by a zero bit. The acknowledge signifies both that a process was able to receive the acknowledged data byte and that the receiving link is able to receive another byte.

Links are not synchronized with **ClockIn** and are insensitive to its phase. Thus links from independently clocked systems may communicate, providing only that the clocks are nominally identical and within specification.

Links are TTL compatible and intended to be used in electrically quiet environments, between devices on a single printed circuit board or between two boards via a backplane. Direct connection may be made between devices separated by a distance of less than 300 millimeters. For longer distances a matched 100 ohm transmission line should be used with series matching resistors **RM**. When this is done the line delay should be less than 0.4 bit time to ensure that the reflection returns before the next data bit is sent.

Buffers may be used for very long transmissions. If so, their overall propagation delay should be stable within the skew tolerance of the link, although the absolute value of the delay is immaterial.

The IMS C011E link supports the standard INMOS communication speed of 10 Mbits/sec. In addition it can be used at 20 Mbits/sec. Link speed can be selected in one of two ways. In Mode 1 it is altered by **SeparateIQ** (page 6). In Mode 2 it is selected by **LinkSpeed**; when the **LinkSpeed** pin is low, the link operates at the standard 10 Mbits/sec; when high it operates at 20 Mbits/sec.

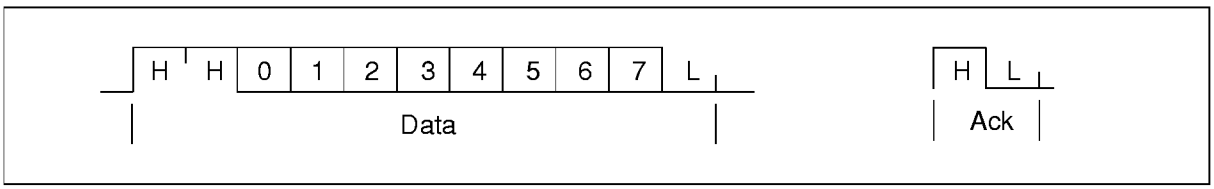


Figure 4.1 IMS C011E link data and acknowledge packets

Symbol	Parameter		Min	Nom	Max	Units	Notes
TJQr	**LinkOut** rise time				25	ns	
TJQf	**LinkOut** fall time				15	ns	
TJDr	**LinkIn** rise time				25	ns	
TJDf	**LinkIn** fall time				20	ns	
TJQJD	Buffered edge delay		0			ns	
TJBskew	Variation in TJQJD	20 Mbits/s			3	ns	1
		10 Mbits/s			10	ns	1
CLIZ	**LinkIn** capacitance	@ f=1MHz			7	pF	
CLL	**LinkOut** load capacitance				50	pF	
RM	Series resistor for 100W transmission line			56		ohms	

Notes

1 This is the variation in the total delay through buffers, transmission lines, differential receivers etc., caused by such things as short term variation in supply voltages and differences in delays for rising and falling edges.

Table 4.1 Link

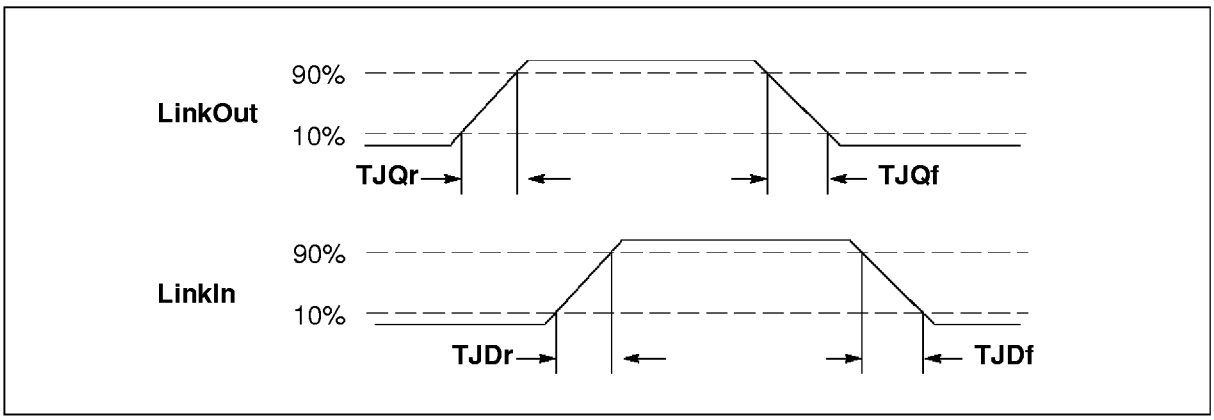


Figure 4.2 IMS C011E link timing

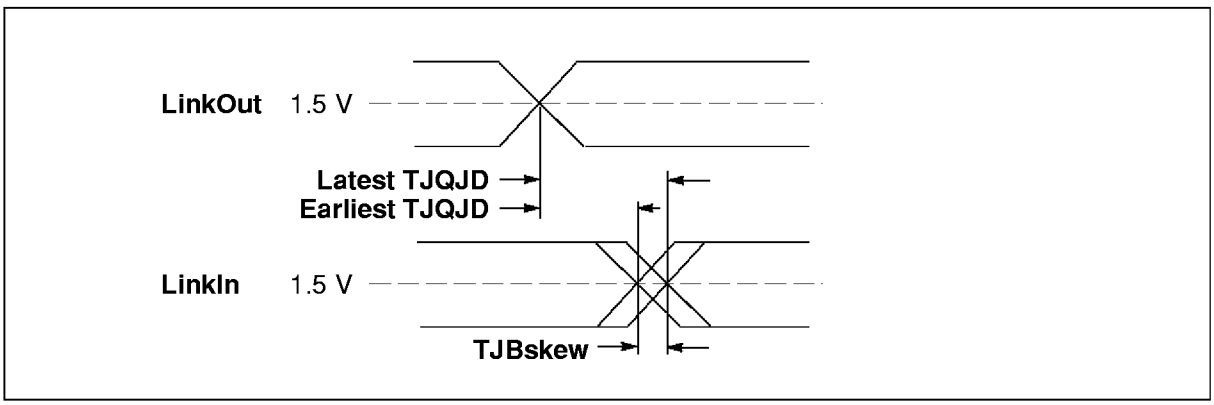


Figure 4.3 IMS C011E buffered link timing

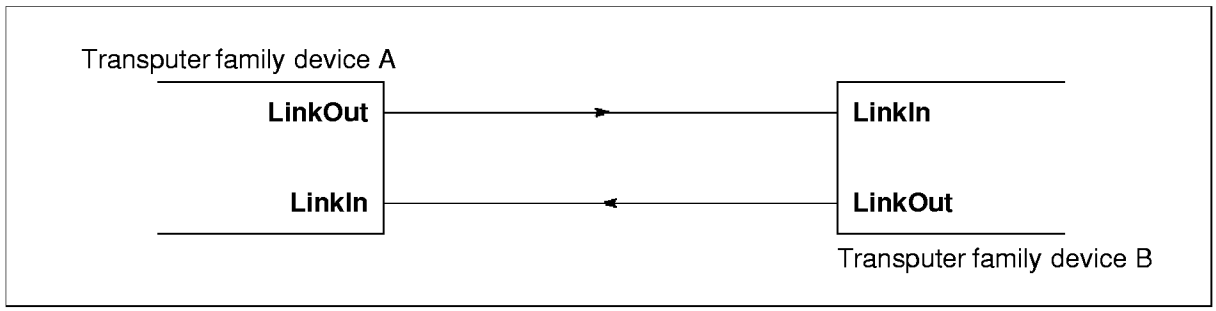


Figure 4.4 Links directly connected

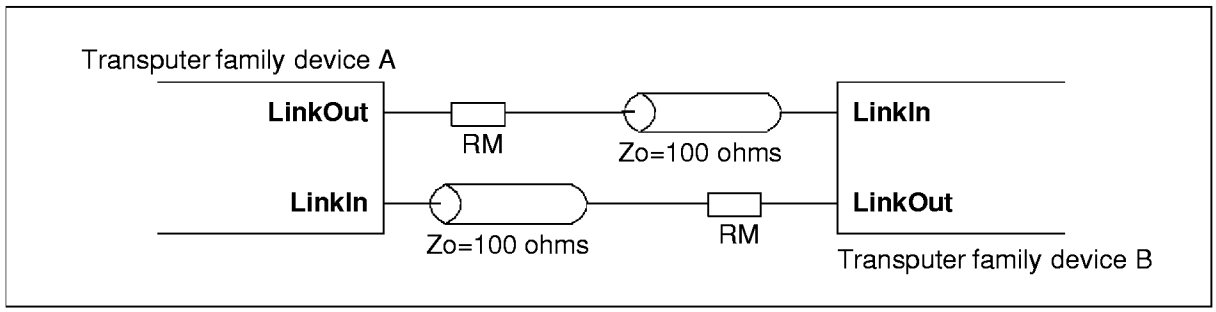


Figure 4.5 Links connected by transmission line

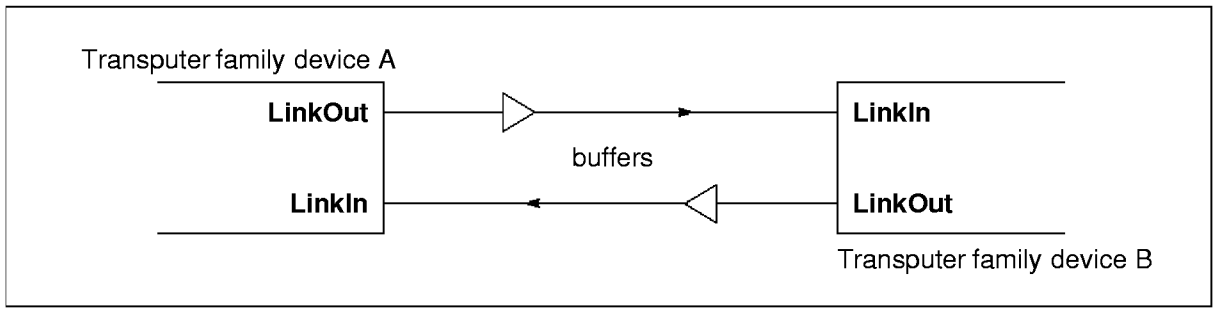


Figure 4.6 Links connected by buffers

5 Mode 1 parallel interface

In Mode 1 the IMS C011E link adaptor is configured as a parallel peripheral interface with handshake lines. Communication with a transputer family device is via the serial link. The parallel interface comprises an input port and an output port, both with handshake.

5.1 Input port

The eight bit parallel input port **I0-7** can be read by a transputer family device via the serial link. **IValid** and **IAck** provide a simple two-wire handshake for this port. When data is valid on **I0-7**, **IValid** is taken high by the peripheral device to commence the handshake. The link adaptor transmits data presented on **I0-7** out through the serial link. After the data byte transmission has been completed and an acknowledge packet is received on the input link, the IMS C011E sets **IAck** high. To complete the handshake, the peripheral device must return **IValid** low. The link adaptor will then set **IAck** low. New data should not be put onto **I0-7** until **IAck** is returned low.

Symbol	Parameter	Min	Nom	Max	Units	Notes
TIdVIvH	Data setup	5			ns	
TIvHLdV	**IValid** high to link data output	0.8		2.5	bits	1,2
TLaVIaH	Link acknowledge start to **IAck** high			3.5	bits	1,3
TIaHIdX	Data hold after **IAck** high	0			ns	
TIaHIvL	**IValid** hold after **IAck** high	0			ns	
TIvLIaL	**IAck** hold after **IValid** low	0.8		3	bits	1
TIaLIvH	Delay before next **IValid** high	0			ns	

Notes

1 Unit of measurement is one link data bit time; at 10 Mbits/s data link speed, one bit time is nominally 100 ns.

2 Maximum time assumes there is no acknowledge packet already on the link. Maximum time with acknowledge on the link is extended by 2 bits.

3 Both data transmission and the returned acknowledge must be completed before **IAck** can go high.

Table 5.1 Mode 1 parallel data input

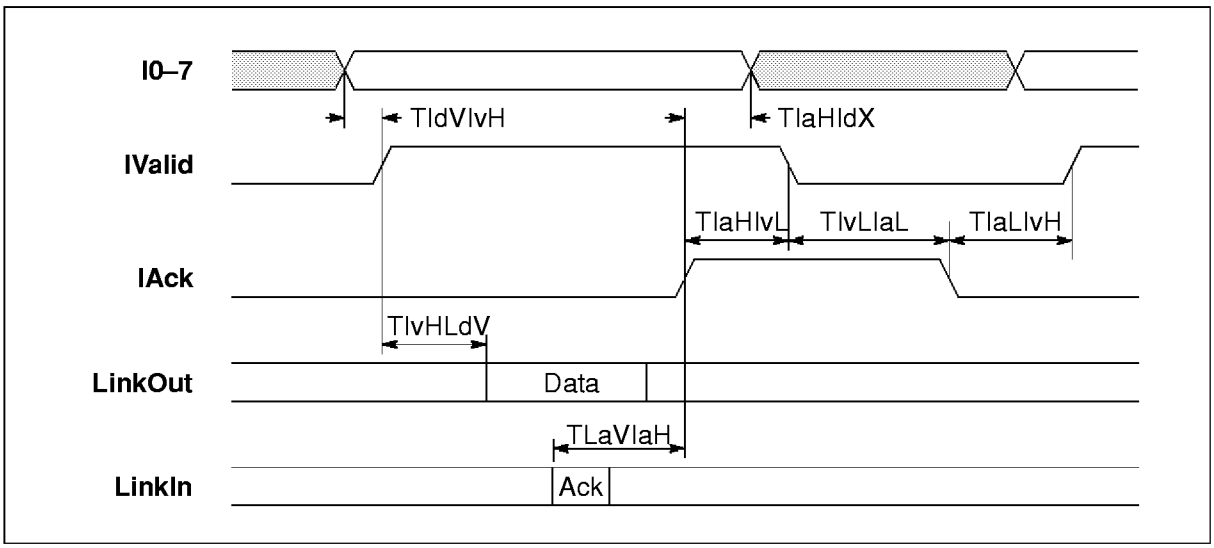


Figure 5.1 IMS C011E Mode 1 parallel data input to link adaptor

5.2 Output port

The eight bit parallel output port **Q0-7** can be controlled by a transputer family device via the serial link. **QValid** and **QAck** provide a simple two-wire handshake for this port.

A data packet received on the input link is presented on **Q0-7**; the link adaptor then takes **QValid** high to initiate the handshake. After reading data from **Q0-7**, the peripheral device sets **QAck** high. The IMS C011E will then send an acknowledge packet out of the serial link to indicate a completed transaction and set **QValid** low to complete the handshake.

Symbol	Parameter	Min	Nom	Max	Units	Notes
TLdVQvH	Start of link data to **QValid**	11.5			bits	1
TQdVQvH	Data setup	15			ns	2
TQvHQaH	**QAck** setup time from **QValid** high	0			ns	
TQaHQvL	**QAck** high to **QValid** low	1.8			bits	1
TQaHLaV	**QAck** high to Ack on link	0.8		2.5	bits	1,3
TQvLQaL	**QAck** hold after **QValid** low	0			ns	
TQvLQdX	Data hold	11			bits	1,4

Notes

1 Unit of measurement is one link data bit time; at 10 Mbits/s data link speed, one bit time is nominally 100 ns.

2 Where an existing data output bit is re-written with the same level there will be no glitch in the output level.

3 Maximum time assumes there is no data packet already on the link. Maximum time with data on the link is extended by 11 bits.

4 Data output remains valid until overwritten by new data.

Table 5.2 Mode 1 parallel data output

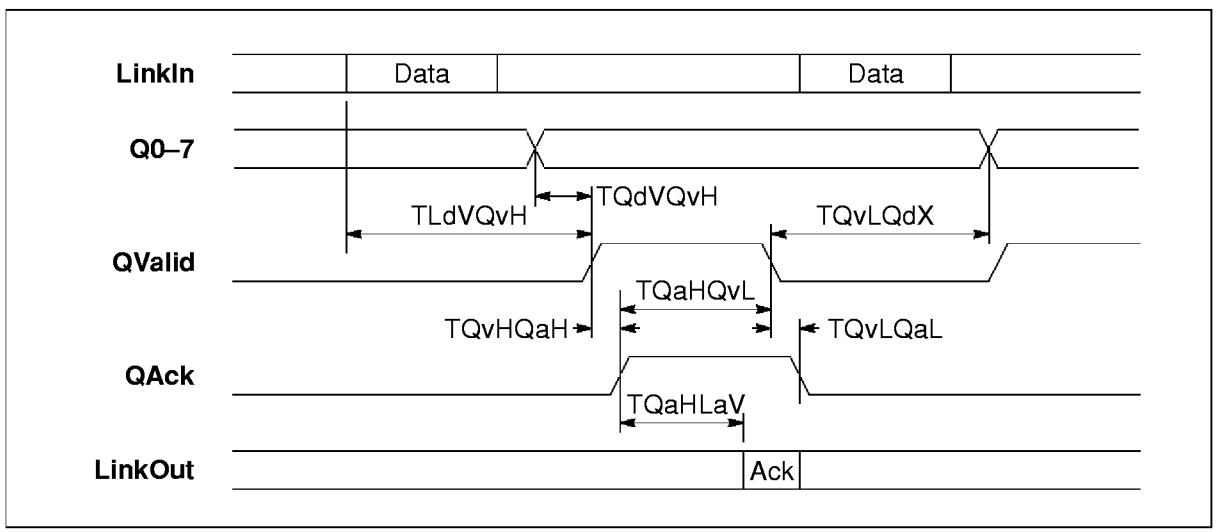


Figure 5.2 IMS C011E Mode 1 parallel data output from link adaptor

6 Mode 2 parallel interface

The IMS C011E provides an interface between a link and a microprocessor style bus. Operation of the link adaptor is controlled through the parallel interface bus lines **D0-7** by reading and writing various registers in the link adaptor. Registers are selected by **RS0-1** and **RnotW**, and the chip enabled with **notCS**.

For convenience of description, the device connected to the parallel side of the link adaptor is presumed to be a microprocessor, although this will not always be the case.

6.1 D0–7

Data is communicated between a microprocessor bus and the link adaptor via the bidirectional bus lines **D0-7**. The bus is high impedance unless the link adaptor chip is selected and the **RnotW** line is high. The bus is used by the microprocessor to access status and data registers.

6.2 notCS

The link adaptor chip is selected when **notCS** is low. Register selectors **RS0-1** and **RnotW** must be valid before **notCS** goes low; **D0-7** must also be valid if writing to the chip (**RnotW** low). Data is read by the link adaptor on the rising edge of **notCS**.

6.3 RnotW

RnotW, in conjunction with **notCS**, selects the link adaptor registers for read or write mode. When **RnotW** is high, the contents of an addressed register appear on the data bus **D0-7**; when **RnotW** is low the data on **D0-7** is written into the addressed register. The state of **RnotW** is latched into the link adaptor by **notCS** going low; it may be changed before **notCS** returns high, within the timing restrictions given.

6.4 RS0–1

One of four registers is selected by **RS0-1**. A register is addressed by setting up **RS0-1** and then taking **notCS** low; the state of **RnotW** when **notCS** goes low determines whether the register will be read or written. The state of **RS0-1** is latched into the link adaptor by **notCS** going low; it may be changed before **notCS** returns high, within the timing restrictions given. The register set comprises a read-only data input register, a write-only data output register and a read/write status register for each.

RS1	RS0	RnotW	Register
0	0	1	Read data
0	0	0	Invalid
0	1	1	Invalid
0	1	0	Write data
1	0	1	Read input status
1	0	0	Write input status
1	1	1	Read output status
1	1	0	Write output status

Table 6.1 IMS C011E Mode 2 register selection

6.4.1 Input Data Register

This register holds the last data packet received from the serial link. It never contains acknowledge packets. It contains valid data only whilst the *data present* flag is set in the input status register. It cannot be assumed to contain valid data after it has been read; a double read may or may not return valid data on the second read. If *data present* is valid on a subsequent read it indicates new data is in the buffer. Writing to this register will have no effect.

Symbol	Parameter	Min	Nom	Max	Units	Notes
TRSVCSL	Register select setup	5			ns	
TCSLRSX	Register select hold	8			ns	
TRWVCSL	Read/write strobe setup	5			ns	
TCSLRWX	Read/write strobe hold	8			ns	
TCSLCSH	Chip select active	65			ns	
TCSHCSL	Delay before re-assertion of chip select	50			ns	

Table 6.2 IMS C011E Mode 2 parallel interface control

Symbol	Parameter	Min	Nom	Max	Units	Notes
TLdVIIH	Start of link data to **InputInt** high			14	bits	1
TCSLIIL	Chip select to **InputInt** low			35	ns	
TCSLDrX	Chip select to bus active	3			ns	
TCSLDrV	Chip select to data valid			55	ns	
TCSHDrZ	Chip select high to bus tristate			38	ns	
TCSHDrX	Data hold after chip select high	3			ns	
TCSHLaV	Chip de-select to start of Ack	0.8		2.5	bits	1,2

Notes

1 Unit of measurement is one link data bit time; at 10 Mbits/s data link speed, one bit time is nominally 100 ns.

2 Maximum time assumes there is no data packet already on the link. Maximum time with data on the link is extended by 11 bits.

Table 6.3 IMS C011E Mode 2 parallel interface read

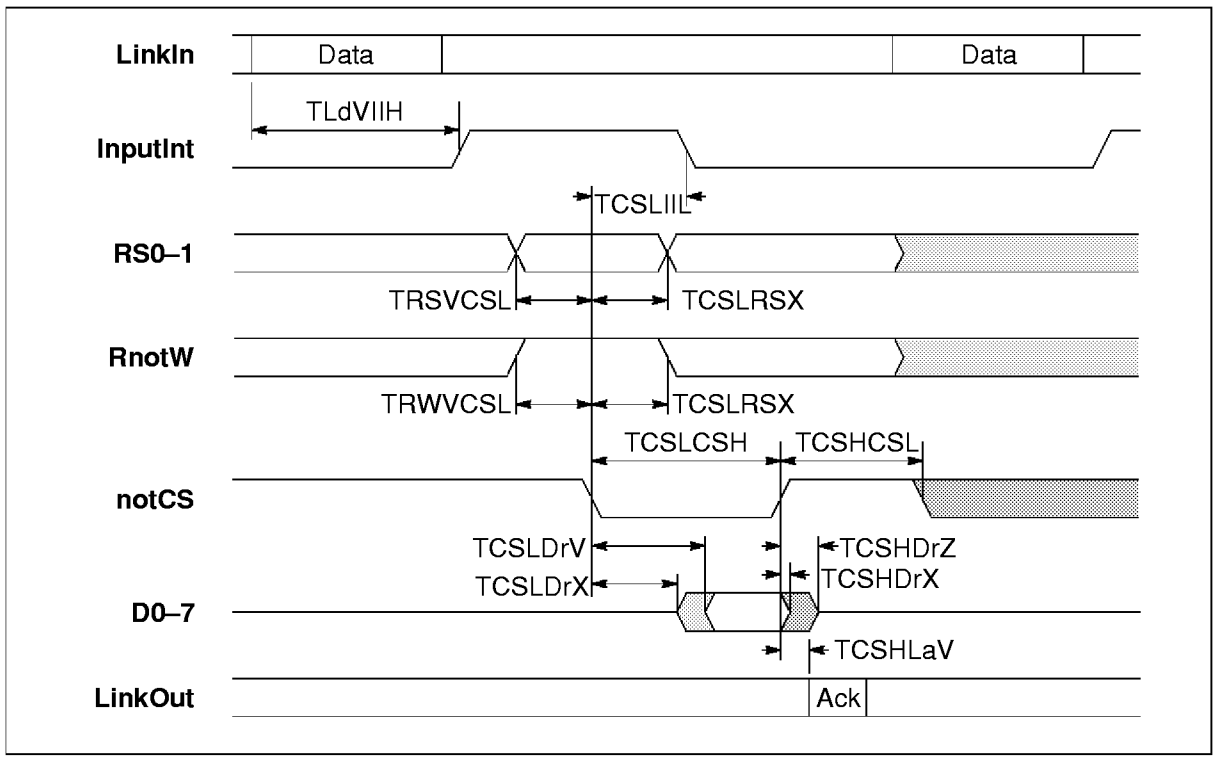


Figure 6.1 IMS C011E Mode 2 read parallel data from link adaptor

Symbol	Parameter	Min	Nom	Max	Units	Notes
TCSHDwV	Data setup	15			ns	
TCSHDwX	Data hold	8			ns	
TCSLOIL	Chip select to **OutputInt** low			35	ns	
TCSHLdV	Chip select high to start of link data	0.8		2.5	bits	1,2
TLaVOIH	Start of link Ack to **OutputInt** high			3.3	bits	1,3
TLdVOIH	Start of link data to **OutputInt** high			13	bits	1,3

Notes

1 Unit of measurement is one link data bit time; at 10 Mbits/s data link speed, one bit time is nominally 100 ns.

2 Maximum time assumes there is no acknowledge packet already on the link. Maximum time with acknowledge on the link is extended by 2 bits.

3 Both data transmission and the returned acknowledge must be completed before **OutputInt** can go high.

Table 6.4 IMS C011E Mode 2 parallel interface write

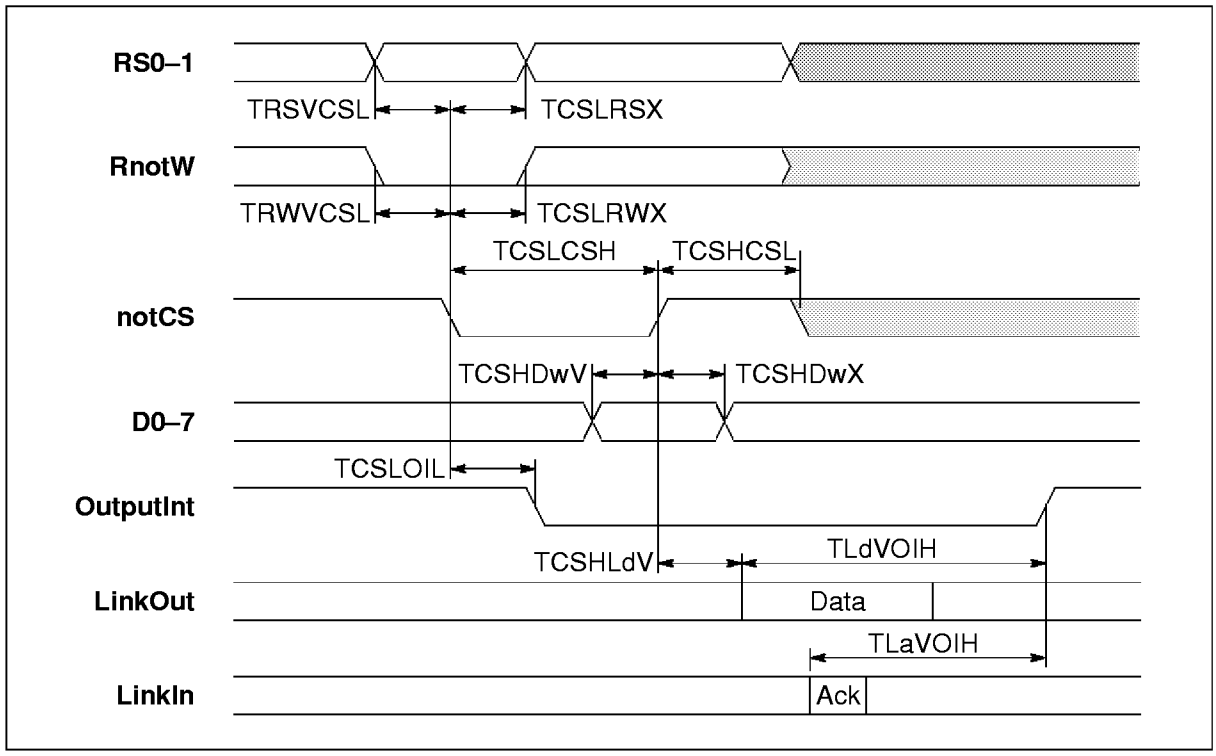


Figure 6.2 IMS C011E Mode 2 write parallel data to link adaptor

6.4.2 Input Status Register

This register contains the *data present* flag and the *interrupt enable* control bit for **InputInt**. The *data present* flag is set to indicate that data in the data input buffer is valid. It is reset low only when the data input buffer is read, or by **Reset**. When writing to this register, the *data present* bit must be written as zero.

The *interrupt enable* bit can be set and reset by writing to the status register with this bit high or low respectively. When the *interrupt enable* and *data present* flags are both high, the **InputInt** output will be high (section 6.5). Resetting *interrupt enable* will take **InputInt** low; setting it again before reading the data input register will set **InputInt** high again. The *interrupt enable* bit can be read to determine its status.

When writing to this register, bits 2-7 must be written as zero; this ensures that they will be zero when the register is read. Failure to write zeroes to these bits may result in undefined data being returned by these bits during a status register read.

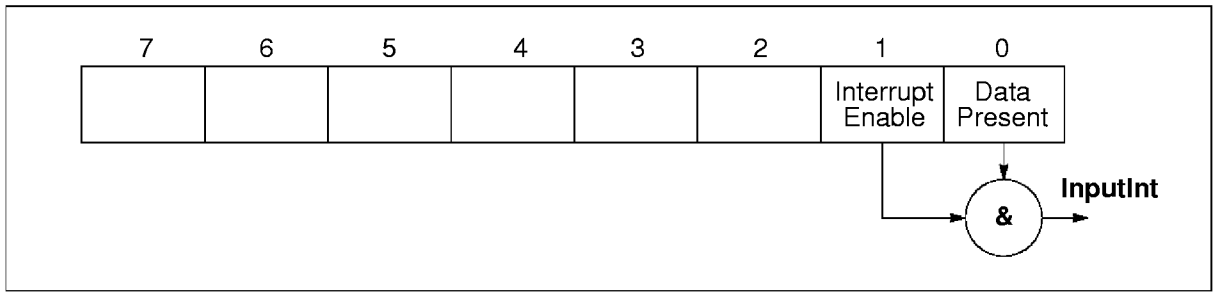


Figure 6.3 IMS C011E Mode 2 input status register

6.4.3 Output Data Register

Data written to this link adaptor register is transmitted out of the serial link as a data packet. Data should only be written to this register when the *output ready* bit in the output status register is high, otherwise data already being transmitted may be corrupted. Reading this register will result in undefined data being read.

6.4.4 Output Status Register

This register contains the *output ready* flag and the *interrupt enable* control bit for **OutputInt**. The *output ready* flag is set to indicate that the data output buffer is empty and a link acknowledge has been received. It is reset low only when data is written to the data output buffer; it is set high by **Reset**. When writing to this register, the *output ready* bit must be written as zero.

The *interrupt enable* bit can be set and reset by writing to the status register with this bit high or low respectively. When the *interrupt enable* and *output ready* flags are both high, the **OutputInt** output will be high (section 6.6). Resetting *interrupt enable* will take **OutputInt** low; setting it again whilst the data output register is empty will set **OutputInt** high again. The *interrupt enable* bit can be read to determine its status.

When writing to this register, bits 2-7 must be written as zero; this ensures that they will be zero when the register is read. Failure to write zeroes to these bits may result in undefined data being returned by these bits during a status register read.

6.5 InputInt

The **InputInt** output is set high to indicate that a data packet has been received from the serial link. It is inhibited from going high when the *interrupt enable* bit in the input status register is low (section 6.4.2). **InputInt** is reset low when data is read from the input data register (section 6.4.1) and by **Reset** (page 7).

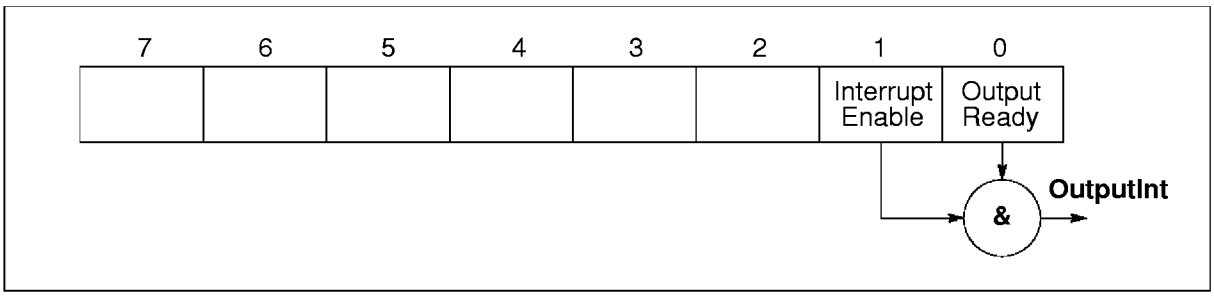


Figure 6.4 IMS C011E Mode 2 output status register

6.6 OutputInt

The **OutputInt** output is set high to indicate that the link is free to receive data from the microprocessor for transmission as a data packet out of the serial link. It is inhibited from going high when the *interrupt enable* bit in the output status register is low (section 6.4.4). **OutputInt** is reset low when data is written to the data output register; it is set low by **Reset** (page 7).

6.7 Data read

A data packet received on the input link sets the *data present* flag in the input status register. If the *interrupt enable* bit in the status register is set, the **InputInt** output pin will be set high. The microprocessor will either respond to the interrupt (if the *interrupt enable* bit is set) or will periodically read the input status register until the *data present* bit is high.

When data is available from the link, the microprocessor reads the data packet from the data input register. This will reset the *data present* flag and cause the link adaptor to transmit an acknowledge packet out of the serial link output. **InputInt** is automatically reset by reading the data input register; it is not necessary to read or write the input status register.

6.8 Data write

When the data output buffer is empty and a link acknowledge has been received the *output ready* flag in the output status register is set high. If the *interrupt enable* bit in the status register is set, the **OutputInt** output pin will also be set high. The microprocessor will either respond to the interrupt (if the *interrupt enable* bit is set) or will periodically read the output status register until the *output ready* bit is high.

When the *output ready* flag is high, the microprocessor can write data to the data output buffer. This will result in the link adaptor resetting the *output ready* flag and commencing transmission of the data packet out of the serial link. The *output ready* status bit will remain low until the data byte transmission has been completed and an acknowledge packet is received by the input link. This will set the *output ready* flag high; if the *interrupt enable* bit is set, **OutputInt** will also be set high.

7 Electrical specifications

7.1 DC electrical characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VDD	DC supply voltage	0	7.0	V	1,2,3
V_I, V_O	Voltage on input and output pins	–0.5	VDD+0.5	V	1,2,3
I_I	Input current		25	mA	4
t_{OSC}	Output short circuit time (one pin)		1	s	2
T_S	Storage temperature	–65	150	°C	2
T_A	Ambient temperature under bias	–55	125	°C	2
P_{Dmax}	Maximum allowable dissipation		600	mW	

Notes

1 All voltages are with respect to **GND**.

2 This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operating sections of this specification is not implied. Stresses greater than those listed may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3 This device contains circuitry to protect the inputs against damage caused by high static voltages or electrical fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than the absolute maximum rated voltages to this high impedance circuit. Unused inputs should be tied to an appropriate logic level such as **VDD** or **GND**.

4 The input current applies to any input or output pin and applies when the voltage on the pin is between **GND** and **VDD**.

Table 7.1 Absolute maximum ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VDD	DC supply voltage	4.75	5.25	V	1
V_I, V_O	Input or output voltage	0	VDD	V	1,2
C_L	Load capacitance on any pin		60	pF	3
T_A	Operating temperature range	–55	125	°C	

Notes

1 All voltages are with respect to **GND**.

2 Excursions beyond the supplies are permitted but not recommended; see DC characteristics.

3 Excluding **LinkOut** load capacitance.

Table 7.2 Operating conditions

SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
V_{IH}	High level input voltage		2.0§	VDD+0.5	V	1,2
V_{IL}	Low level input voltage		–0.5	0.8	V	1,2
I_I	Input current	@ GND<VI<VDD		10	mA	1,2,3
				200	mA	1, 2, 4
V_{OH}	Output high voltage	@ IOH=2mA	VDD–1		V	1,2
V_{OL}	Output low voltage	@ IOL=4mA		0.4	V	1,2
I_{OZ}	Tristate output current	@ GND<V0<VDD		10	mA	1,2
P_D	Power dissipation			150	mW	2, 5
C_{IN}	Input capacitance	@ f=1MHz		7	pF	
C_{OZ}	Output capacitance	@ f=1MHz		10	pF	
§For **RnotW**, **RS0-1**, **SeparateIQ** over temperature range –55 <**TA**<25°C substitute 2.2V.						

Notes

1 All voltages are with respect to **GND**.

2 Parameters for IMS C011E measured at 4.75V<**VDD**<5.25V and –55°C<**TA**<125°C.

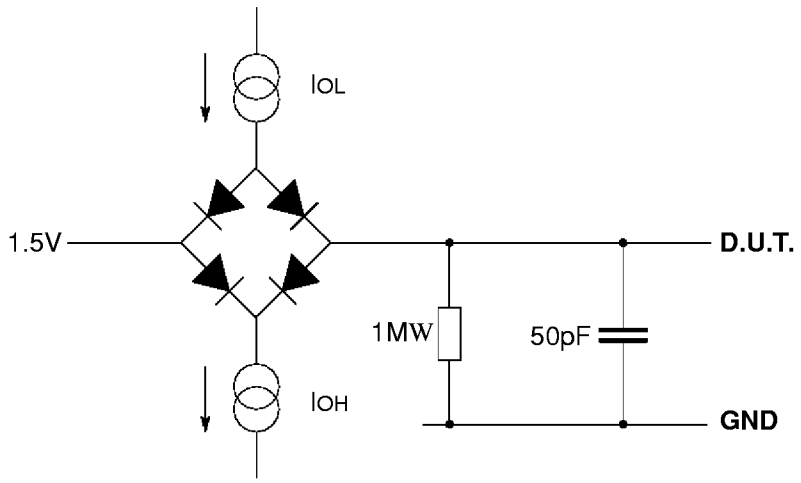
3 For inputs other than those in Note 4.

4 For pins 2, 3, 5, 6, 7, 9, 11, 13, 15, 16, 25.

5 Power dissipation varies with output loading.

Table 7.3 DC characteristics

7.2 Equivalent circuits



Note: This circuit represents the device sinking IOL and sourcing IOH with a 50pF capacitive load.

Figure 7.1 Load circuit for AC measurements

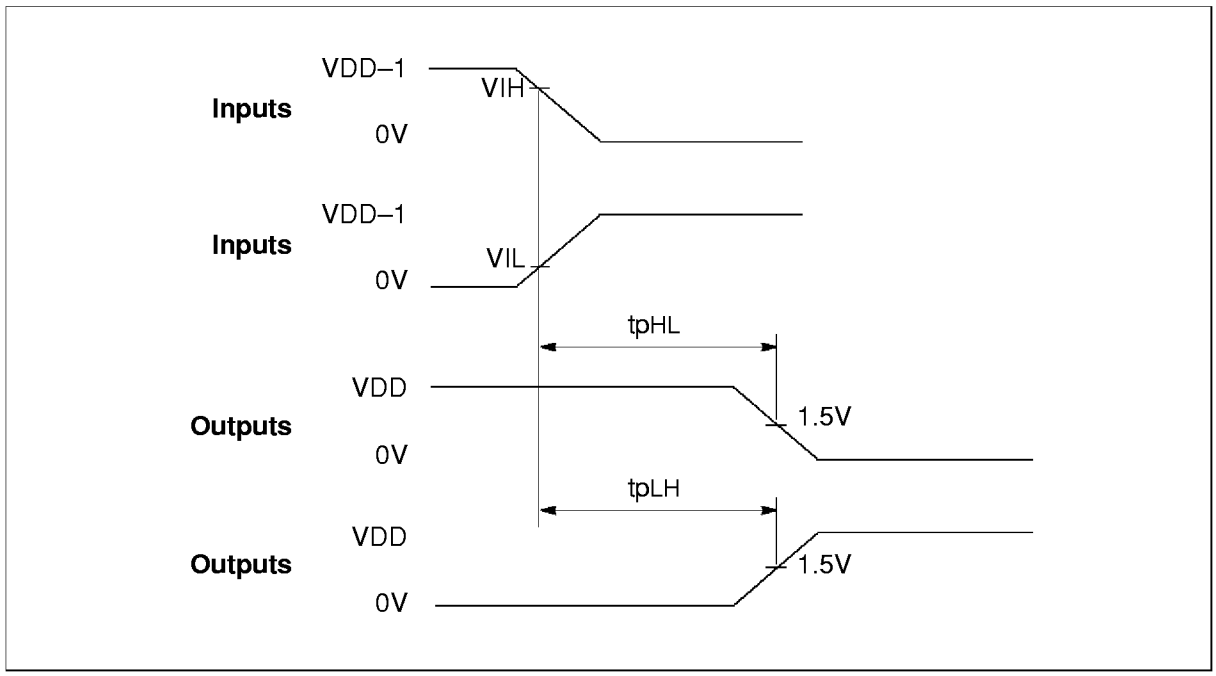


Figure 7.2 AC measurements timing waveforms

7.3 AC timing characteristics

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
TDr	Input rising edges	2	20	ns	1, 2
TDf	Input falling edges	2	20	ns	1, 2
TQr	Output rising edges		38	ns	1
TQf	Output falling edges		20	ns	1

Notes

1 Non-link pins; see section on links.

2 All inputs except **ClockIn**; see section on **ClockIn**.

Table 7.4 Input and output edges

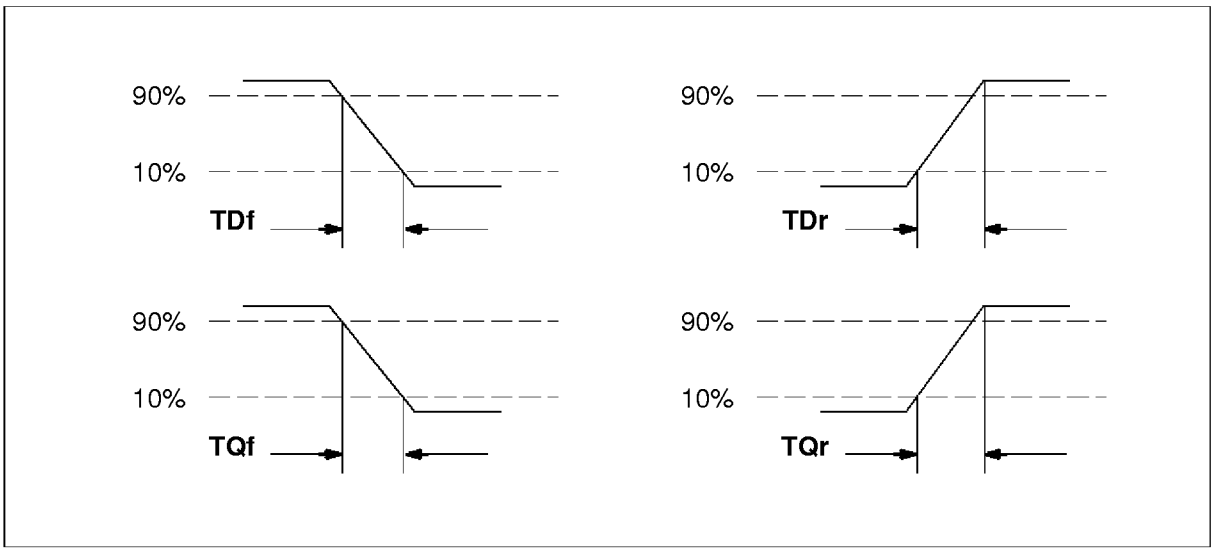


Figure 7.3 IMS C011E input and output edge timing

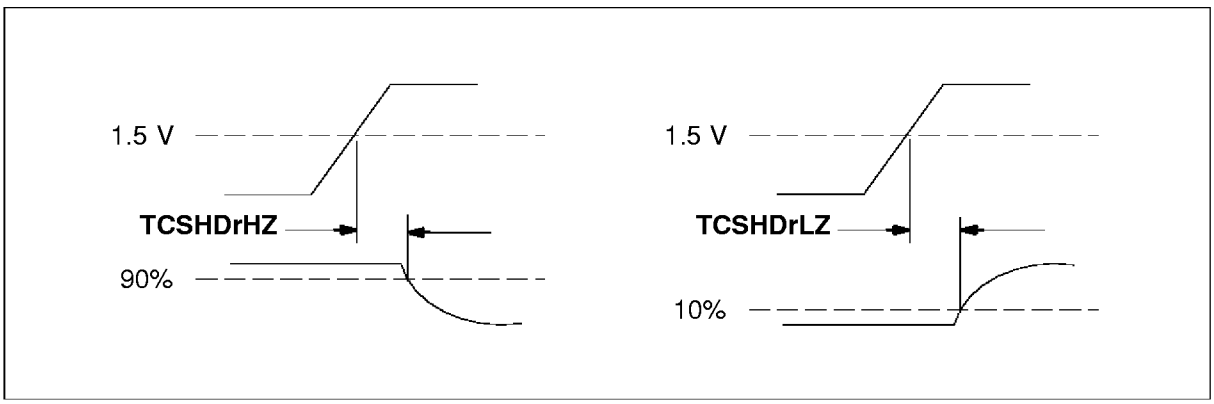


Figure 7.4 IMS C011E tristate timing relative to **notCS**

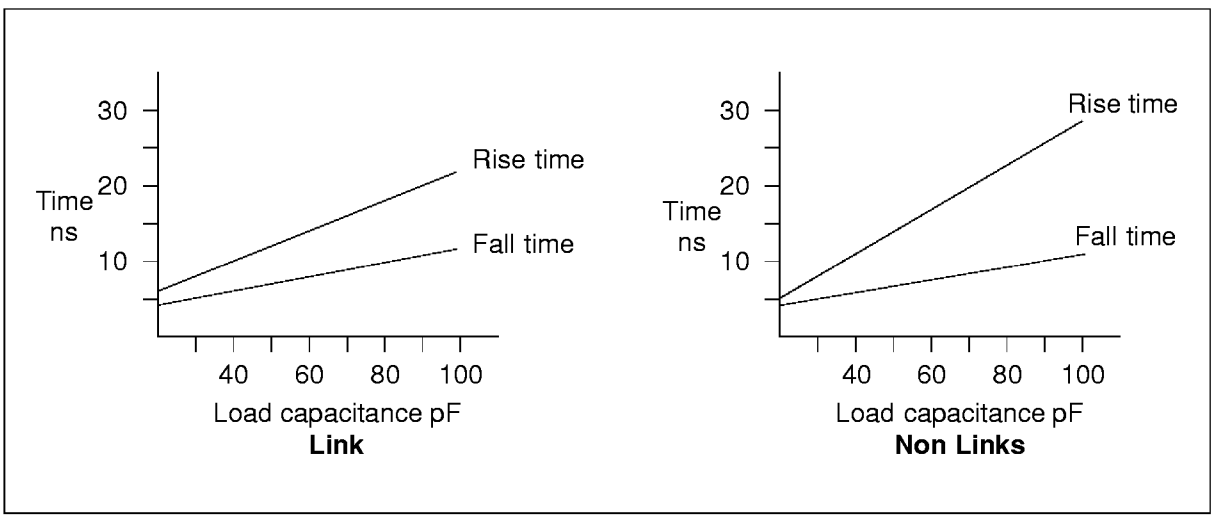


Figure 7.5 Typical rise/fall times

7.4 Power rating

Internal power dissipation (P_{INT}) of transputer and peripheral chips depends on **VDD**, as shown in figure 7.6. P_{INT} is substantially independent of temperature.

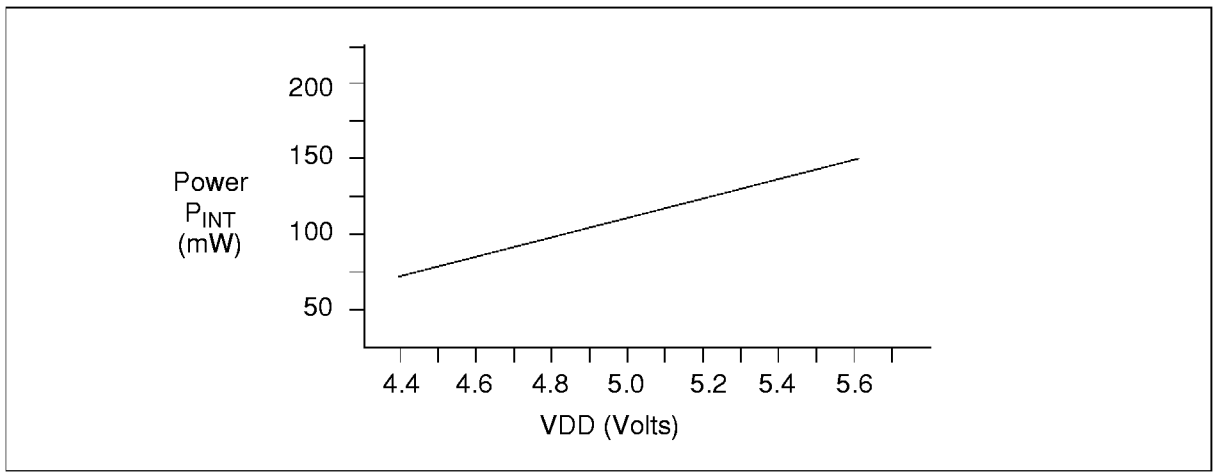


Figure 7.6 IMS C011E internal power dissipation vs VDD

Total power dissipation (P_D) of the chip is

$$P_D = P_{INT} + P_{IO}$$

where P_{IO} is the power dissipation in the input and output pins; this is application dependent.

Internal working temperature T_J of the chip is

$$T_J = T_A + q_{JA} * P_D$$

where T_A is the external ambient temperature in °C and q_{JA} is the junction-to-ambient thermal resistance in °C/W.

Further information about device thermal characteristics can be found in section 8.5.

8 Package specifications

The IMS C011E is available in 28-pin ceramic dual-in-line (DIL) and 28-pin ceramic leadless chip carrier (LCC) packages.

8.1 28 pin ceramic DIL package pinouts

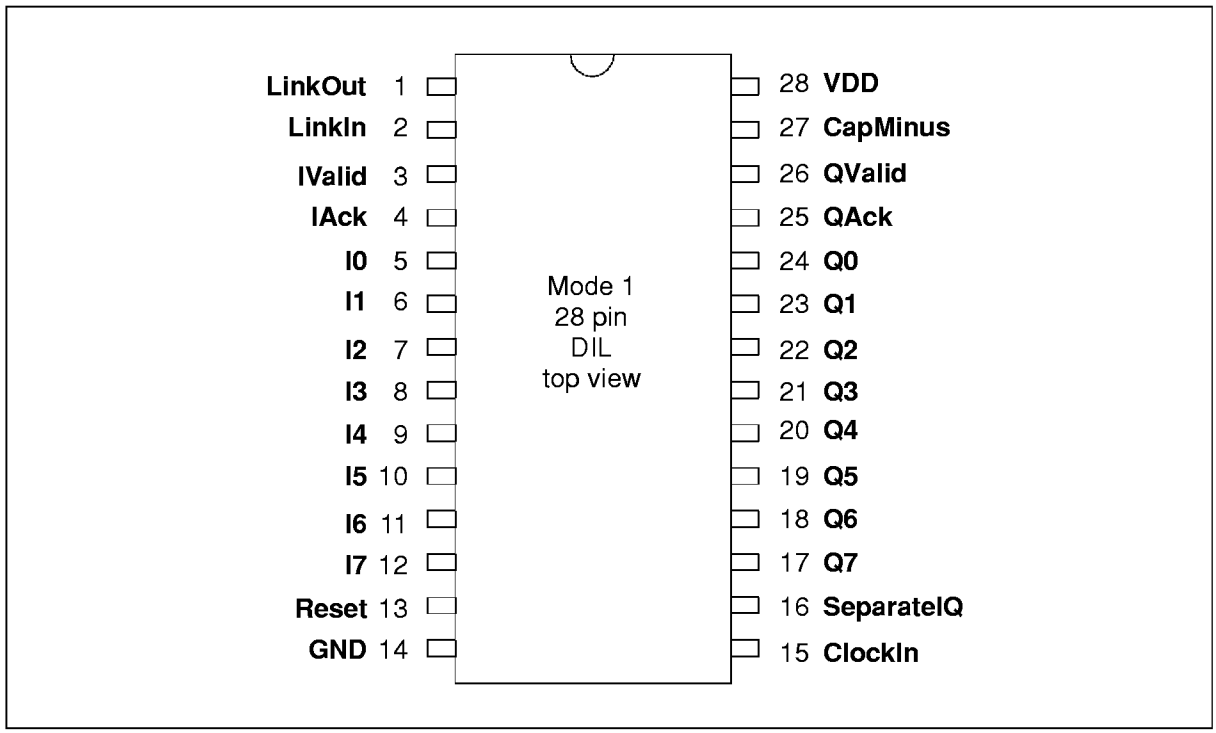


Figure 8.1 IMS C011E **Mode 1** 28 pin DIL package pinout

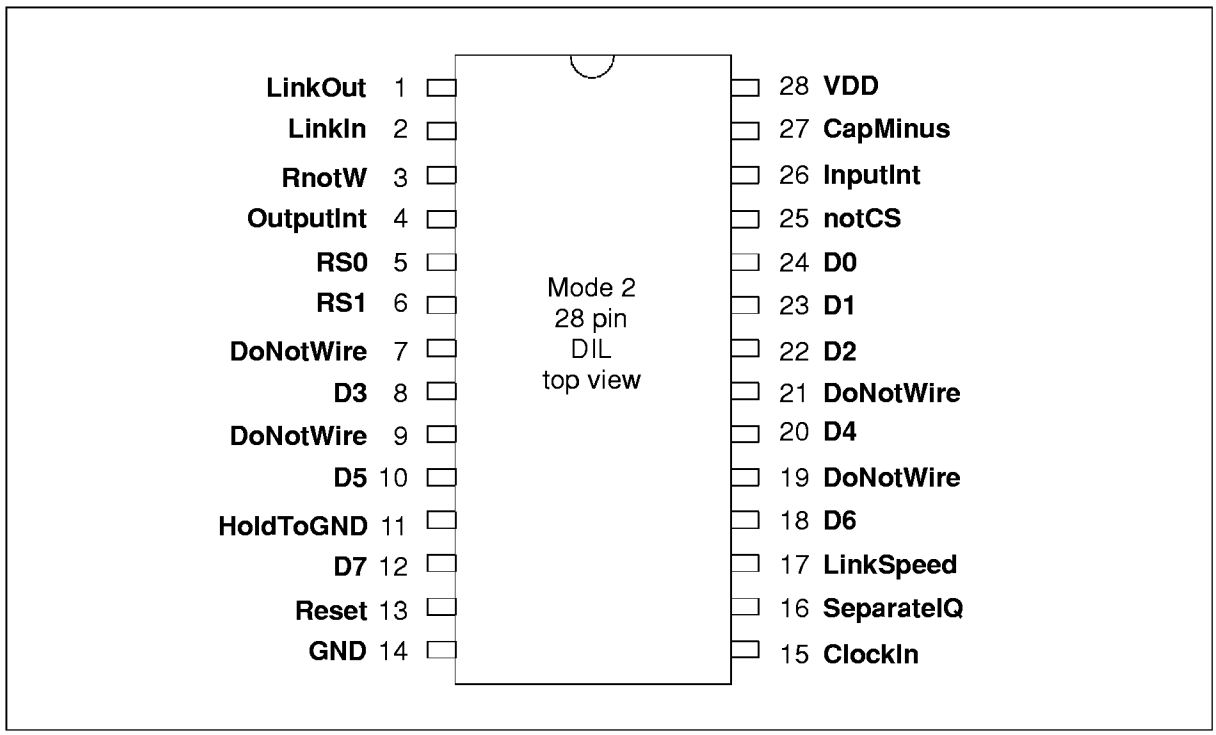


Figure 8.2 IMS C011E **Mode 2** 28 pin DIL package pinout

8.2 28 pin ceramic dual-in-line (DIL) package dimensions

DIM	CONTROL DIMENSIONS INCH			ALTERNATIVE DIMENSIONS mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	–	–	0.167	–	–	4.242
A1	0.040	–	–	1.016	–	–
A2	0.085	–	0.107	2.159	–	2.718
B	0.014	0.018	0.022	0.356	0.457	0.559
B1	–	0.060TYP	–	–	1.524TYP	–
C	0.008	0.010	0.012	0.203	0.254	0.305
D	1.386	1.420	1.436	35.204	36.068	36.474
E	0.605	–	0.625	15.367	–	15.875
E1	0.585	–	0.605	14.859	–	15.367
e	–	0.100BSC	–	–	2.540BSC	–
e3	–	1.300BSC	–	–	33.020BSC	–
L	0.125	–	0.165	3.175	–	4.191

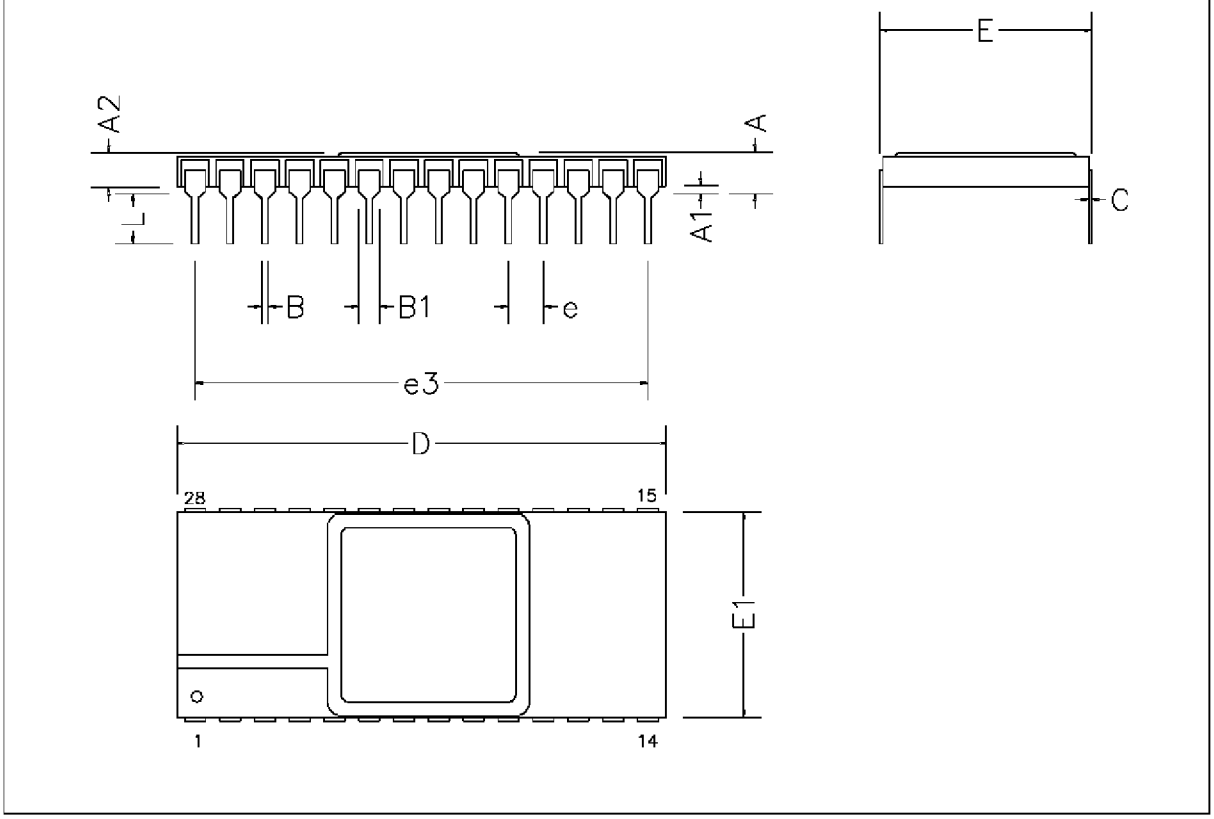


Figure 8.3 28 pin ceramic dual-in-line package dimensions

8.3 28 pin ceramic LCC package pinouts

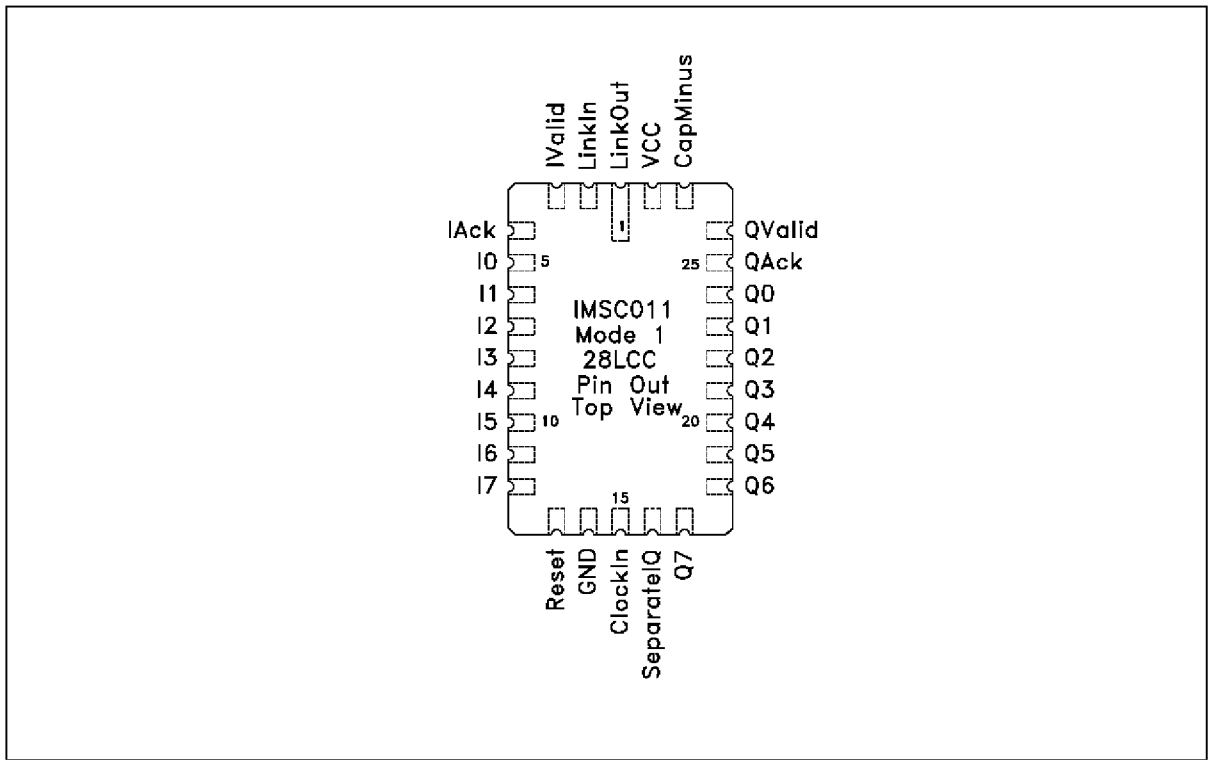


Figure 8.4 IMS C011E **Mode 1** 28 pin LCC package pinout

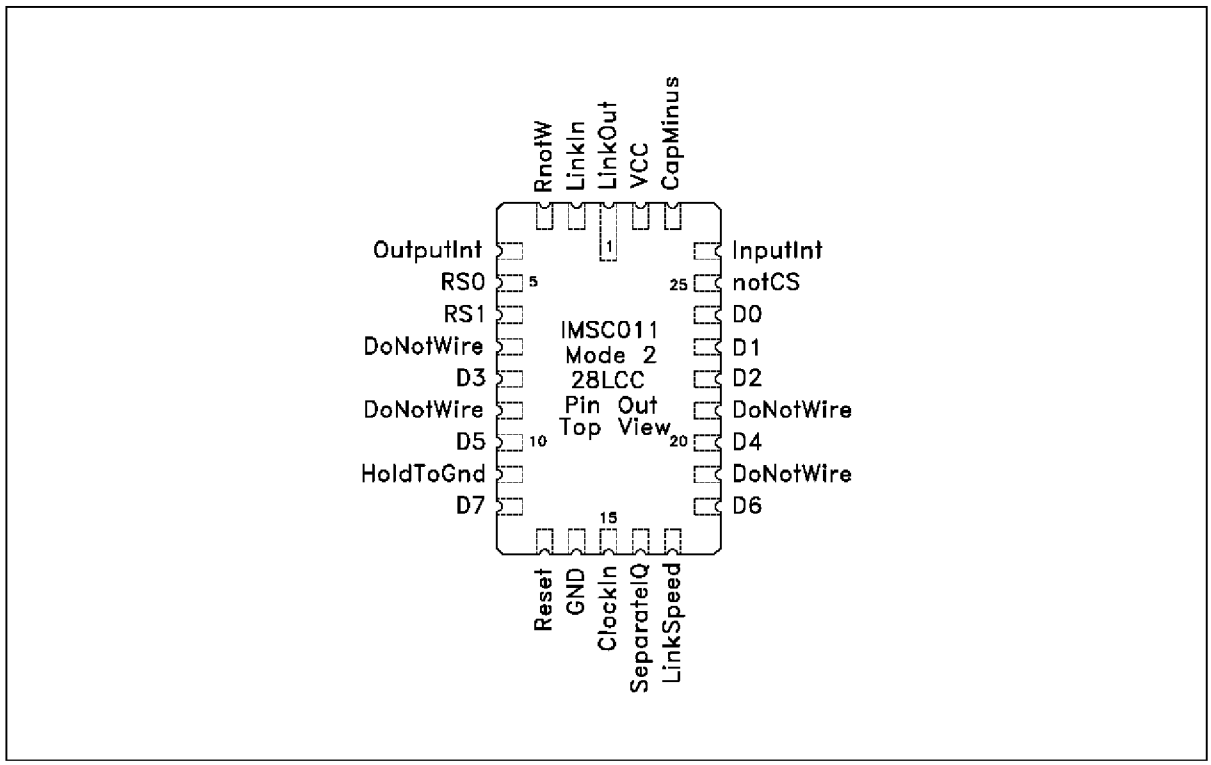


Figure 8.5 IMS C011E **Mode 2** 28 pin LCC package pinout

8.4 28 pin ceramic leadless chip carrier (LCC) package dimensions

	Inches		Millimetres	
DIM	Min	Max	Min	Max
A	0.064	0.078	1.625	1.981
B1	0.022	0.028	0.559	0.711
D	0.540	0.560	13.716	14.224
E	0.340	0.360	8.636	9.144
e1	0.048	0.052	1.219	1.321

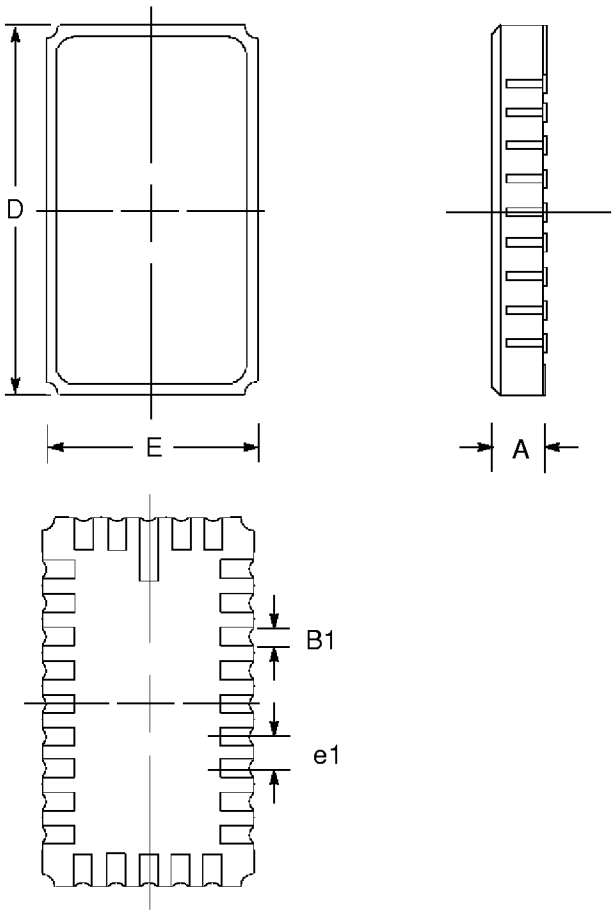


Figure 8.6 28 pin leadless chip carrier package dimensions

8.5 Thermal specification

The IMS C011E is tested to a maximum silicon temperature of 140_C. For operation within the given specifications, the case temperature should not exceed 135_C.

For temperatures above 135_C the operation of the device cannot be guaranteed and reliability may be impaired.

For further information on reliability refer to the SGS–THOMSON Microelectronics Quality and Reliability Program.

9 Ordering

This section indicates the designation of package selections for the IMS C011E. Speed of **ClockIn** is 5MHz for all parts.

For availability contact your local SGS–THOMSON sales office or authorized distributor.

SGS–THOMSON designation	Package
IMS C011-S20E	28 pin ceramic dual-in-line
IMS C011-N20E	28 pin ceramic LCC

Table 9.1 IMS C011E ordering details